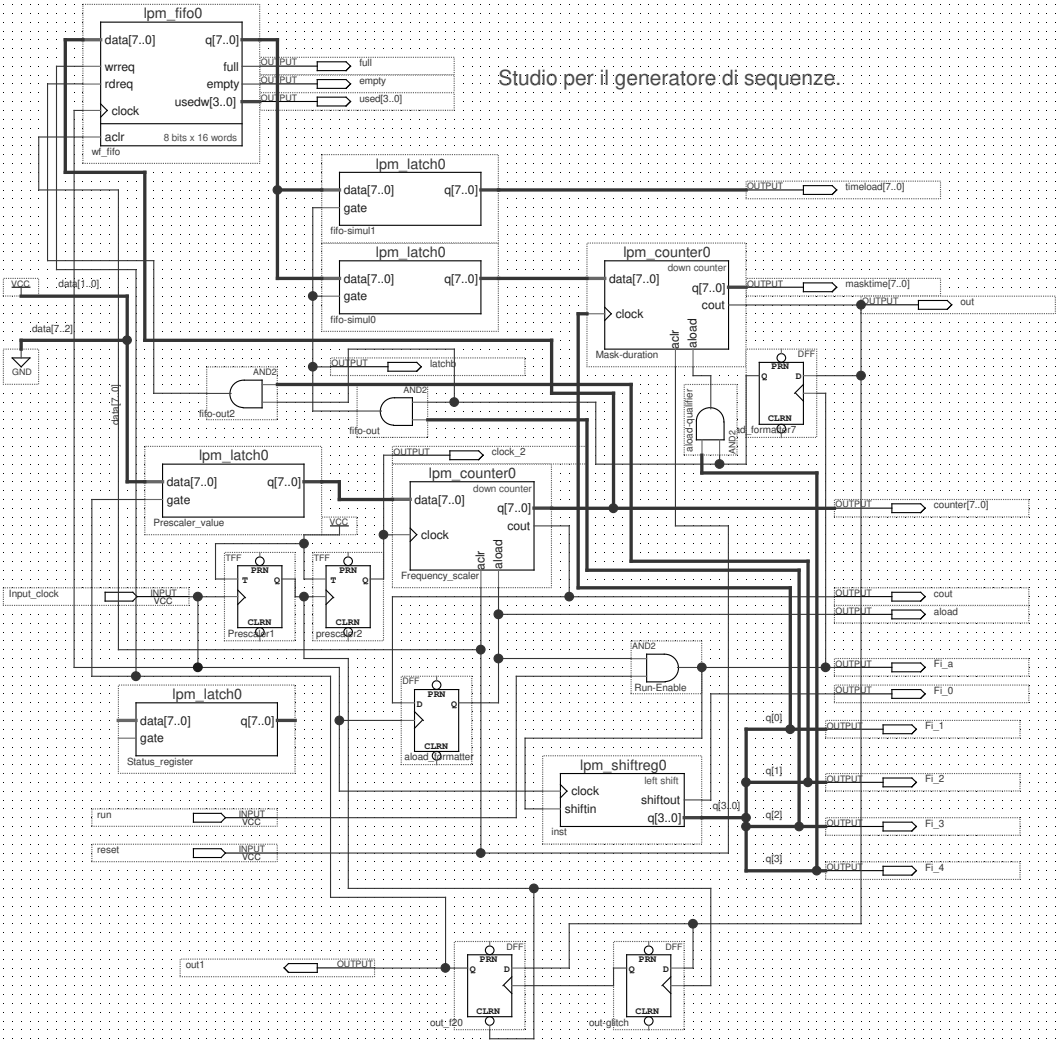
Studio per il generatore di sequenze
lpm_fifo0
data[7..0]
q[7..0]
wrreq
full
rdreq
empty
usedw[3..0]
clock
aclr
8 bits x 16 words
wf_fifo
OUTPUT
full
empty
used[3..0]
lpm_latch0
data[7..0]
q[7..0]
gate
fifo-simul1
fifo-simul0
timeload[7..0]
lpm_counter0
down counter
cout
masktime[7..0]
out
Mask-duration
aclr
aload
VCC
GND
data[3..0]
data[7..2]
latch0
AND2
fifo-out2
fifo-out
aload-qualifier
DFF
PRN
CLRN
ad_formatter
clock_2
Prescaler_value
Frequency_scaler
counter[7..0]
TFF
T
Q
Input_clock
INPUT
Prescaler1
prescaler2
cout
aload
Run-Enable
Fi_a
Fi_0
Fi_1
Fi_2
Fi_3
Fi_4
Status_register
aload_formatter
lpm_shiftreg0
left shift
clock
shiftin
shiftout
q[3..0]
inst
run
reset
out1
out_f20
out_glitch